An Audio Regulator Dynamic Tester

Walt Jung

This brief note focuses on an audio regulator dynamic test method, which applies a pulse load to a working Super Regulator (SR) It allows examining the resulting transient error across the output. This is especially useful towards determining dynamic stability for various degrees of capacitive loading. Or, to determine regulation impedance.

Figure 1 is a working setup. Under test here is a "SR2020" positive regulator, similar in many regards to the *Audio-Electronics* issue 4/2000 "SR" circuit. **[1]** In the present case it is vintage 2020, thus SR2020.

Figure 1: A Dynamic Regulator Test

The external DC load on this (+) 13.7V test regulator is ~60mA. Dynamic AC loading of the tester is ~100mA (peak). The tester circuit is on the breadboard foreground.

Note that the tester is *hard soldered to the Vout Force/Sense terminals*, using #18 short solid wires. AC sensing is done via the 100Ω resistor and the flexible red wire to *Vout Force/Sense*. The dynamic tester load current is returned to *Vout Force/Sense* nodes via smaller enamel wires.

Test capacitors are plugged into the Vout node 0.1" female pins, or similar pins on the tester (yellow arrows mark these sockets). This provides contrast between local/remote loads. Electrically, this is in parallel to C4 on the regulator PCB. The test cap is denoted as "C4R".

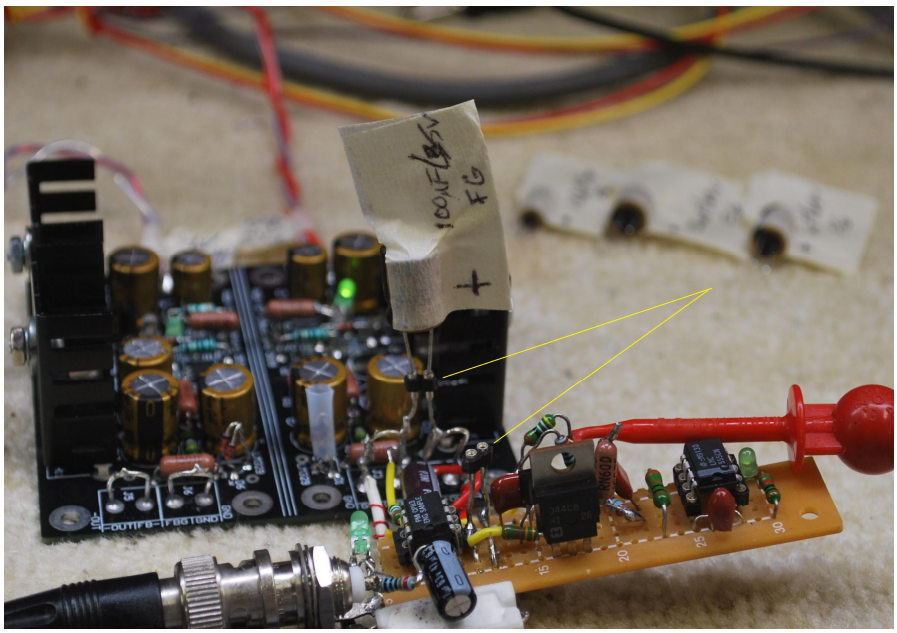
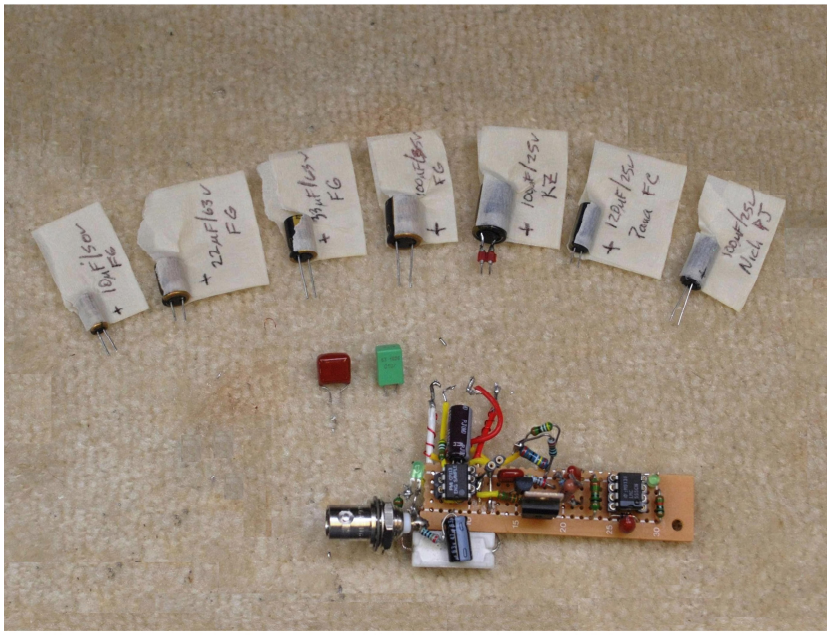


Table 1: C4R Capacitor Types Tested

C4R	Vendor	Series	Catalog #
10uF/50V	Nichicon	FG	UFG1H100MDM
22uF/63V	Nichicon	FG	UFG1J220MPM
33uF/63V	Nichicon	FG	UFG1J330MPM
100uF/35V	Nichicon	FG	UFG1V101MPM
100uF/25V	Nichicon	KZ	UKZ1E101MPM
100uF/25V (not tested)	Panasonic	FC	EEU-FC1E101SB
120uF/25V (tested)	Panasonic	FC	EEU-FC1E121 (obsolete)
100uF/25V	Nichicon	PJ	UPJ1E101MED

Figure 2: The Array of Caps Tested

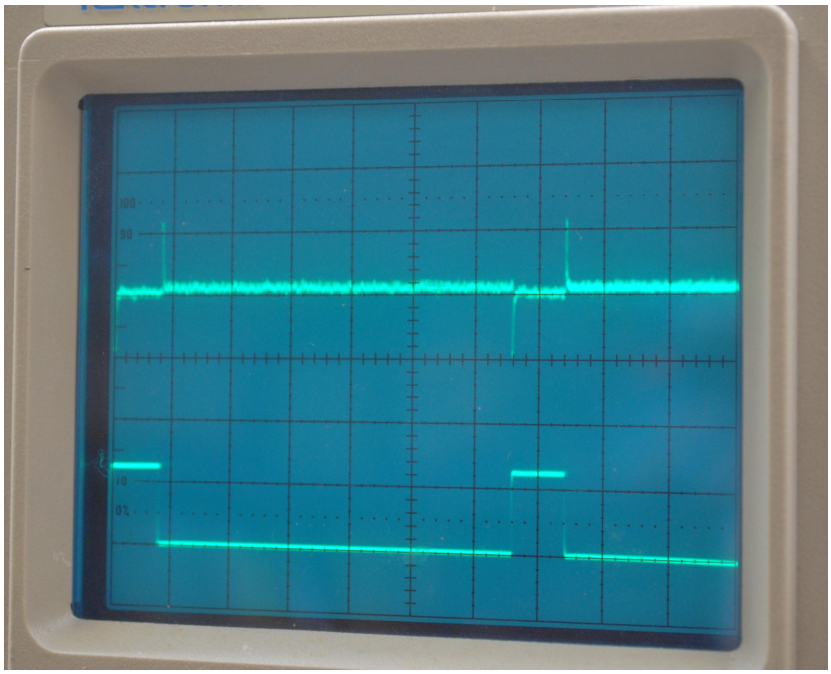


The array of electrolytic caps tested are shown in the top row of the picture at the left. They correspond to those listed as C4R within *Table 1*.

The prototype tester is shown in the foreground, disconnected from the regulator.

A pair of high-Q film caps are also shown for reference, in the middle. Either of these cap types, stacked film or box style, could (and did) introduce in-stability. They are shown here only to emphasize the point that they should* not *be used!

Figure 3: Dynamic Test Waveforms



Within the as-tested circuit board assembly, the electrolytics used are all from the Nichicon FG series: 22uF/63V (1) at Vraw input, and 100uF/35V elsewhere (3). Here a 100uF/35V cap is under test at C4R (as yellow-highlighted in *Table 1*). Note that the PCB C4 is removed for these tests.

Upper Trace:

The Vout AC waveform Verr. as seen directly at the +/- sense points. The vertical scale is 10mV / major division, and after the tester preamp 100x AC gain, the effective scope display is 100µV / div.

Lower Trace:

SR2020 regulator drive. Positive peak corresponds to 100mA AC load.

Discussion:

The tester uses a combination of techniques to make the low-level error signal apparent. The 0.1A step current is one. With a regulator Zout of ≤ 1milliohm, an AC gain of 100x preamp was used for these tests.

Figure 3 above shows the error voltage of the test regulator in the upper trace, with a step load change of

100mA (lower trace). The pulse risetime is controlled at ~10µs, consistent with audio bandwidths. Artifacts are the residual wideband baseline noise, mostly the AD825 op amp input noise. There are also narrow transient switching spikes. The spikes appear in all the readings taken, but are considered benign, as real audio signals likely won't have 10µs risetimes. See more on this under the **Spikes:** section.

Interestingly, with all the capacitors shown in the upper row of ***Fig. 2*****,** the *Vout AC error voltage waveform varied little*. Thus, it is considered pointless to show all of them here. This factor suggests that the transient errors displayed are not a strong function of the capacitor type, so much as it is of the intrinsic regulator impedance. This makes intuitive sense, as the tested capacitors generally have an ESR of 100 or more times the regulator Zout.

The P-P regulator error voltage Verr is barely perceptible on the 100µV/ major division scale of ***Fig. 3***, where the minor divisions correspond to 20µV. The stepped portion is of primary interest, and it is roughly a trace width, i.e., ~20 µV or so. Since Zout can be computed as Verr/I, this would correspond to an impedance of ~0.0002 Ω (or ~200 µΩ).

Allowing for various uncertainties, this is roughly consistent with the expected error voltage for a 0.1A load step and an AD825-based regulator. If we assume a regulator open loop Zout of 1Ω and an op amp open loop gain of 6500 (76dB), the expected closed loop Zout should be around 1/6500, or 154 µΩ. While this is in the correct ballpark, one should also say this is not a precise measurement.

An important feature of the observed error voltage is that it is flat, with no overshoot or ringing. Various other electrolytics were tested by insertion into the PCB test jack, and to simplify, *none of them caused any serious aberrations — no overshoots, and no ringing.* No instability was noted, suggesting that the exact type of electrolytic is not extremely critical. As a guideline, the 100uF/25V Nichicon KZ and 100uF/35V Nichicon FG types have a typical 100kHz ESR between 150 and 200mΩ. Either of these families can be recommended.

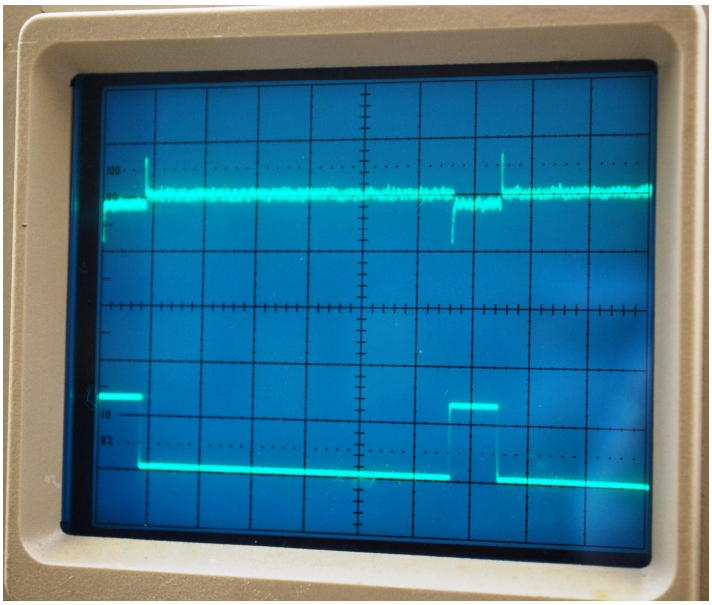
Past capacitor tests have noted that 100-120uF types with 25V (or more) voltage ratings are suitable for these regulator circuits. **[2]** Bear with us on this — the summaries of this old letter seem on point, even after many years. It should not be necessary to repeat the above dynamic load tests with other (modern) electrolytics, so long as they fall within a window for ESR. We suggest a threshold of caution here, namely a 100kHz ESR of not less than 100 mΩ. In the other way, higher ESR is generally OK, so long as it does not exceed about an ohm. For example, a more general-purpose Nichicon 100uF/25Vfrom the UPJ series **[3]** was also tested in one PCB build (four locations) and worked well. This unit has a 100kHz ESR of 0.39Ω. A summary of the electrolytic cap types used at test location C4R is shown in ***Table 1.*** This not an all-inclusive list, by any means.

Spikes:

Looking into the narrow spikes as shown in ***Fig. 3***, these are related to the risetime of the test signal used. The error voltage for this rise/fall period has a greater rate of change, and the regulator produces a higher amplitude, narrow spike to track the signal slope. ***Figure 4*** opposite shows the error voltage (upper trace) of a second test regulator, again with a step load change of 100mA (lower trace). As in ***Fig. 3***, the pulse risetime is controlled at ~10µs. This is test condition ***(A).*** Here the amplitude of the narrow spikes can be seen to be ~80µV. Within the tester, the capacitor controlling rise and fall times is 1nF (same conditions as in the ***Fig. 1*** tests). The lower frequency rectangular portion of this waveform is like ***Fig. 3***.

Figure 5 shows the error voltage (upper trace) of the same regulator with a step load change of 100mA . The pulse risetime is now ~20µs., double that of condition ***(A)***. This is test condition ***(B),*** and the amplitude of the spikes reduce to ~40µV, indicating the regulator is better able to track the slower signal.

Figure 4: Test Waveform Spikes (A)



A second assembled SR2020 PCB was also tested, to explore the spikes. In this setup, the electrolytics used are all from Nichicon FG and KZ series: A 22uF/63V FG (1) at Vraw input, and 100uF/25V KZ types elsewhere (4). This test *(A)* was otherwise like the *Fig. 1* conditions.

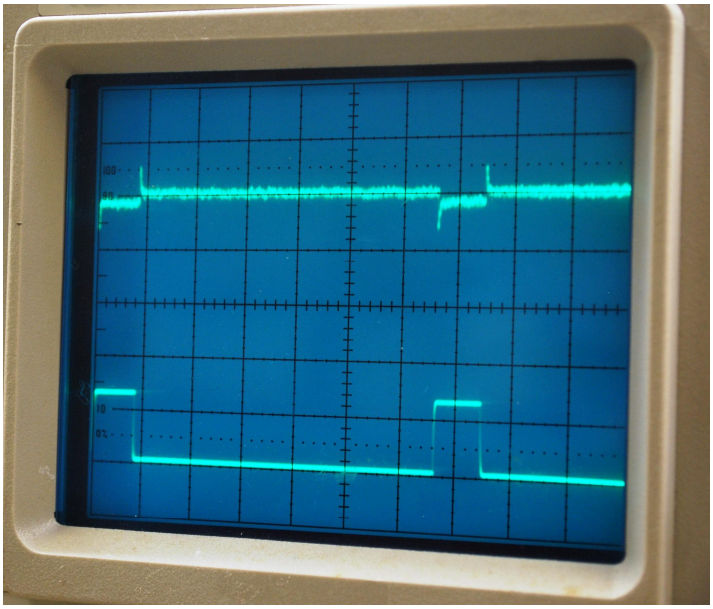
Upper Trace:

The Vout AC waveform Verr. with tester preamp 100x AC gain, and effective scope display of 100µV / div. *Note spike amplitude of ~80µV.*

Lower Trace:

SR2020 regulator drive, 100mA AC load. *Note relatively fast risetime*.

Figure 5: Test Waveform Spikes (B)



In this same SR2020 PCB, a second test *(B)* was performed with the risetime capacitance doubled. This test was otherwise like the *Fig. 4* conditions.

Upper Trace:

The Vout AC waveform Verr. with tester preamp 100x AC gain, and effective scope display of 100µV / div. *Note lower spike amplitude of ~40µV.*

Lower Trace:

SR2020 regulator drive, 100mA AC load. *Note relatively slow risetime.*

Caveats:

This tester involves very low-level signals, and it requires incredibly careful construction to provide meaning. Thus, it is *not* a project for the inexperienced. This "Preview" tester writeup was a preview of this project. This version is updated to include the schematic, shown here as ***Figure 6***.

References:

[1] https://refsnregs.waltjung.org/Improved_PN_Regs.pdf

[2] https://refsnregs.waltjung.org/CAP_LTEs_060620.pdf

[3] https://www.mouser.com/_/?Keyword=UPJ1E101MED&bws=1

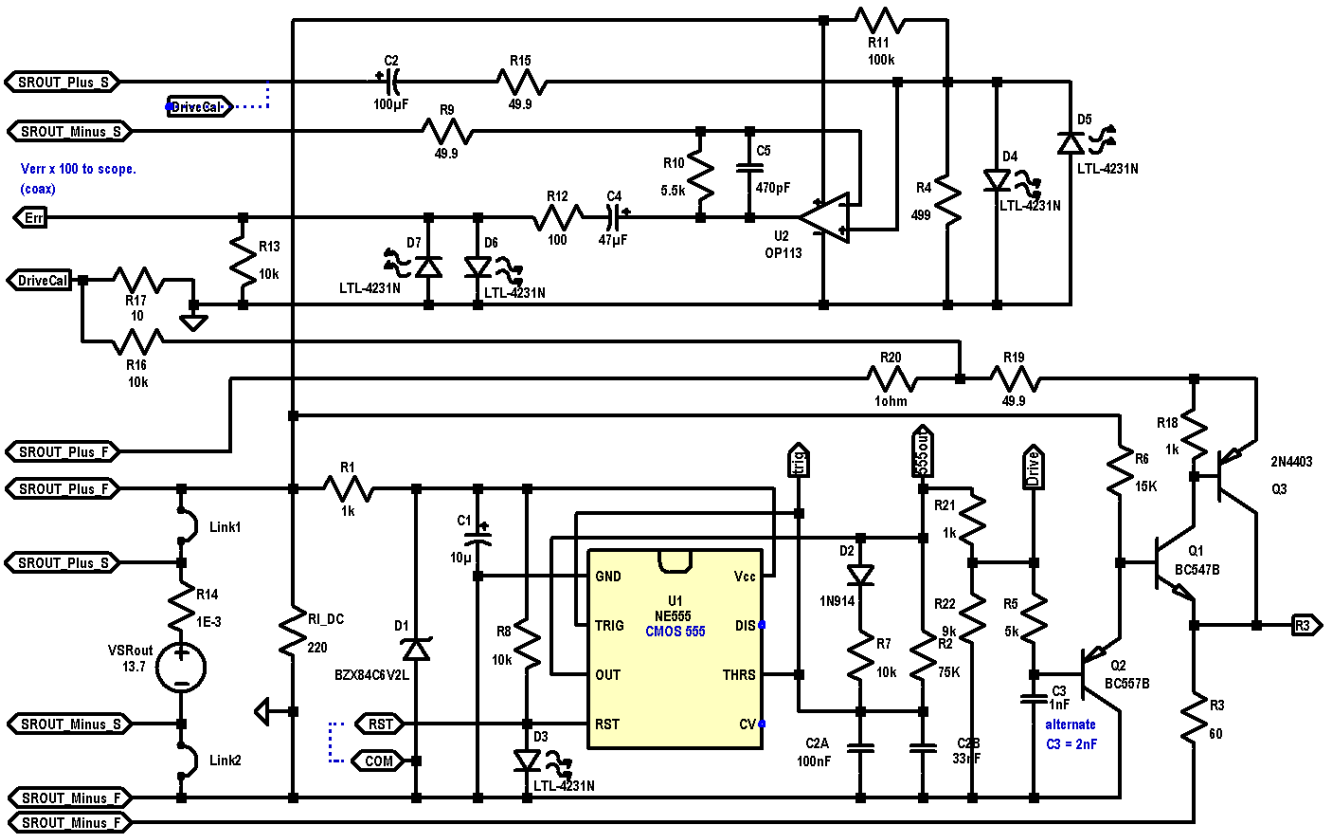


Figure 6: SR2020 Dynamic Load Tester Schematic

The tester is powered by the regulator under test (here shown as VSROut). It provides fixed DC loading (RL_DC), plus a dynamic load (Q3). A high gain low noise preamp (U2) provides a fixed gain of 100 times. A U1 CMOS 555 timer provides the drive at 555out, and an RC network shapes the drive to a controlled risetime as seen across C3.

Notes:

The preamp gain for signal Verr (AC) is: R4/(R4+R15) * (R10+R9)/R9 * R13/(R13+R12). This reduces to 0.909 * 111 * 0.99, or ~ 100x as shown. DC clamping LEDs protect U2 during transients, as well as the monitor scope input.

VSRout is an SR2020 ckt with a DC impedance of R14, or ≤1milliohm. The DC loading of the tester is Vsrout/ RL_DC, or about 13.7 / 220 as shown.

The AC pulse loading is Vdrive / R3, about 100mA. The R3 value is trimmed so that 100mA is present through sense resistor R20 (see DriveCal below).

The low duty cycle pulse has a 10us risetime and occurs at ~1kHz. Pulse width is ~1ms. An alternate C3 (2nF) doubles the risetime.

DriveCal is the reference calibration pulse to the monitor scope. For calibration, connect the C2 (+) terminal to the DriveCal node. Adjust the 10k trimmer (R21 and R22) for ~6V P-P across R3. Then, adjust the R3 value such that DriveCal P-P amplitude = 100uV. With 100x gain of the AC preamp, the scope will display 1 division on a 100uV / division scale. This provides a known 100mA drive to 1% sense resistor R20.